REMARKS

Applicants respectfully request reconsideration of this application in view of the foregoing amendments and the following remarks.

Claim Status

Claims 1-18 are pending in this application. Claims 1-3, 5-9 and 13-18 have been rejected. Claims 4 and 10-12 have been objected to by the Examiner. Claims 2 and 4 are canceled. Claims 1, 3, 5, 9, 11 and 17 are herein amended. No new matter has been added by these amendments.

Objections to the Drawings

Figs. 1 and 2 have been objected to as failing to comply with 37 C.F.R. § 1.84(p)(5) because they include the following reference characters not found in the specification: "R" and "Q1" of Fig. 1; and "Q4" – "Q6" of Fig. 2. Corrected drawings or an amendment to the specification have been required by the Examiner.

Applicants have amended the specification to include the reference characters shown in Figs. 1 and 2. Accordingly, reconsideration of the objections to the drawings is respectfully requested.

Objections to the Specification

The specification has been objected to because of two informalities.

First, the Examiner objected to the use of "passive resistance" on line 12 of page 1 alleging that it should state "active resistance". Applicants have thus amended the specification to recite "active resistance". Reconsideration of this objection is respectfully requested.

Second, the Examiner objected to the sentence "The source of ... PMOS transistor Q13" on page 8, lines 12-13, stating that is should be deleted because Fig. 3 "clearly shows the gate of Q13 being connected to the drain of Q8, and ... that particular gate/source relationship is already described on lines 10-11". Although the Examiner is correct in stating that Fig. 3 shows the gate of the transistor Q13 connected to the drain of the transistor Q8, Applicants disagree with the Examiner's assertion that the sentence be deleted because Fig. 3 also shows the source of the transistor Q13 connected to its gate. As such, reconsideration of this objection is respectfully requested.

Objections to the Claims

Claim 11 has been objected to because as presently written the limitation "a sum of voltages each ... corresponding one" (emphasis added) is believed by the Examiner to be confusing. Claim 11 has been amended to recite, "...wherein the enable voltage is higher than a sum of voltages, wherein each voltage is ~~being~~ obtained between drain and source electrodes of a corresponding one of the plurality of MOS transistors." Reconsideration of this objection is respectfully requested.

Rejections Under 35 U.S.C. § 112

Claim 17 and its dependent claim 18 have been rejected under 35 U.S.C. § 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which Applicants regard as the invention. In particular, the Examiner asserted that the limitations on lines 3-5 of claim 17 are misleading and/or inaccurate and has requested clarification thereof.

Applicants have amended claim 17 to recite "... a voltage supply circuit having at least one PMOS transistor and a set of NMOS transistors, wherein a gate of the PMOS

transistor is connected to the drain of the first MOS transistor, a source of the PMOS transistor receives the externally applied voltage and is connected to ~~a~~ the gate of the PMOS transistor ..." thus clarifying the limitations at issue. If the Examiner needs further clarification regarding these limitations, Applicants direct the Examiner to Figs. 3 and 5, both of which show a gate of a PMOS transistor (e.g., transistors Q13 and Q31) connected to its source.

Claim 9 has been rejected under 35 U.S.C. § 112 because the limitation "MOS transistor" lacks antecedent basis. Claim 9 has been amended to depend from claim 8 thus providing sufficient antecedent basis for the limitation.

As such, Applicants believe that claims 9, 17 and 18 satisfy the requirements of 35 U.S.C. § 112. Accordingly, reconsideration of the rejections is respectfully requested.

Rejections Under 35 U.S.C. § 102

Claims 1, 2, 5-9 and 13-15 have been rejected under 35 U.S.C. § 102(b) as being anticipated by PCT WO 01/61430 A1 (Viehmann).

Applicants respectfully acknowledge the Examiner's indication that claim 4 would be allowable if rewritten in independent form to include the limitations of its base claims and any intervening claims. Accordingly, Applicants have essentially incorporated the features of claims 3 and 4 into independent claim 1 to place independent claim 1 (and the claims which depend therefrom) in condition for allowance.

Applicants have amended claims 3 and 5 to bring them into conformity with amended claim 1 from which they depend.

With regard to independent claim 6 the Examiner indicated that Viehmann shows a "current mirror circuit 20,18 having first/second current paths 30,24,22/32,26 formed

between [a] first power source terminal U_{DD} and a second source terminal (e.g., ground), wherein the current mirror circuit is operated in response to a voltage level of the second current path" and wherein a "reference voltage output node on the second current path (between 32 and 26) provides a reference voltage ... and [an] active resistance device 22, on the first current path, is operated in the linear region". Thus, according to the Examiner claim 6 is anticipated. Applicants respectfully disagree.

Claim 6 of the present invention recites,

> A reference voltage generating circuit comprising:
> a current mirror circuit having first and second current paths formed between a first power source terminal and a second power source terminal, the current mirror circuit being operated in response to a voltage level of the second current path;
> a reference voltage output node for providing a reference voltage, the reference voltage output node being located on the second current path; and
> an active resistance device formed on the first current path to be operated in a linear region of a current-voltage characteristic curve of the active resistance device.

Viehmann, on the other hand, discloses a voltage current transformer having a first current mirror containing two transistors such that under identical drive conditions the current flowing through the first transistor is greater than the current flowing through the second transistor by a predetermined factor. In particular, the voltage current transformer includes the first current mirror, a second current mirror and a MOSFET. Viehmann, does not, however, disclose a reference voltage output node for providing a reference voltage as recited in claim 6 of the present invention.

Instead, Viehmann discloses the first and second current mirrors each having a current path (e.g., an input current path and an output current path). The input current path proceeds from a supply voltage at the second current mirror through the first current

mirror and the MOSFET to ground. The output current path proceeds from the supply voltage at the second current mirror through the first current mirror to ground. There is no reference voltage node for providing a reference voltage along either current path.

Accordingly, the present invention as recited in claim 6 is patentably distinct and not anticipated by Viehmann for at least the reasons stated above.

Rejections Under 35 U.S.C. § 103(a)

Claims 1-3, 5-9 and 13-16 have been rejected under 35 U.S.C. § 103 as being unpatentable over Applicants' admitted prior art (APA), i.e., Fig. 2, in view of what would have been obvious to one of ordinary skill in the art.

Independent claim 1 (and the claims which depend therefrom) are believed to be allowable for at least the reasons discussed above.

With regard to independent claims 6 and 16, and in particular claim 16, the Examiner indicated that the APA discloses a "current mirror circuit" that receives an externally applied voltage "made up of first and second MOS transistors [Q4 and Q5]", a "current control circuit" made up of "third and fourth MOS transistors [Q4 and Q5]" and a "[passive] resistance circuit R". According to the Examiner, "it would have been obvious to one of ordinary skill in the art to replace [the] resistance circuit R with at least one (a fifth) MOS transistor as a means to allow adjustment to the circuit". Thus, "the fifth MOS transistor would function as an active resistance circuit, and since it would be coupled to ground, [it] would typically be an NMOS transistor [rendering claims 6 and 16 obvious]". Applicants respectfully disagree.

Claim 16 of the present invention recites,

> A reference voltage generating circuit comprising:

> a current mirror circuit having first and second MOS transistors, sources of the first and second MOS transistors receiving an externally applied voltage, a gate of the first MOS transistor being connected to a gate of the second MOS transistor and to a drain of the first MOS transistor;
>
> a current control circuit having third and fourth MOS transistors, a drain of the third MOS transistor being connected to the drain of the first MOS transistor, a drain of the fourth MOS transistor being connected to a gate of the third MOS transistor and a drain of the second MOS transistor, a source of the fourth MOS transistor being connected to a ground, and a reference voltage being provided on a node between the drain of the second MOS transistor and the drain of the fourth MOS transistor; and
>
> an active resistance circuit having a fifth MOS transistor, a drain of the fifth MOS transistor being connected to a gate of the fourth MOS transistor and a source of the third MOS transistor, a source of the fifth MOS transistor being connected to the ground, and a gate of the fifth MOS transistor receives a control voltage higher than a voltage between the drain and source of the fifth MOS transistor so that the fifth MOS transistor is operated in a linear region.

The APA is a conventional mirror type reference voltage generating circuit having a passive resistance device. In particular, the device includes several transistors and a resistor. The resistor, which is a passive resistance device, is required for generating a reference voltage and for minimizing the current consumption of the circuit. The APA does not disclose nor suggest using an active resistance device such as a MOS transistor in place of its resistor.

Instead, it appears that the Examiner is using impermissible hindsight reconstruction to modify the APA in view of what would have been obvious to one of ordinary skill in the art. Applicants respectfully assert that obviousness cannot be established by combining the teachings of the APA with what would have been obvious to one of ordinary skill in the art without some proper prior art teaching or suggestion

supporting such a combination. The APA reference does not teach or suggest such a combination. As such, Applicants believe that the invention as recited in claims 6 and 16 is patentable over the cited art of record.

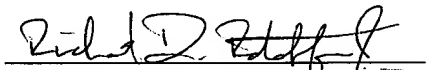
Dependent Claims

Applicants have not independently addressed the rejections of the dependent claims because Applicants submit that, in view of the amendments to the claims presented herein and, for at least similar reasons as why the independent claims from which the dependent claims depend are believed allowable as discussed, supra, the dependent claims are also allowable. Applicants however, reserve the right to address any individual rejections of the dependent claims should such be necessary or appropriate.

CONCLUSION

Accordingly, Applicants submit that the claims as herein presented are allowable over the prior art of record, taken alone or in combination, and that the respective rejections be withdrawn. Applicants further submit that the application is hereby placed in condition for allowance which action is earnestly solicited.

Respectfully submitted,

By: 

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